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EXAMINER	
JOHNSON, BRIAN P	
ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,016	ZHAO ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-18 have been examined.

Acknowledgement of papers filed: amendments and remarks filed 18 March 2009. These papers filed have been placed on record.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title appears to refer to submitting overlapping commands in a pipeline processor. It is noted that most every pipeline processor is capable of this. To assist in further searches, Examiner suggests amending the title to more particularly indicate the novelty of the invention.

Claim Objections

1. Objection is withdrawn in light of Applicant's amendments.

Claim Rejections - 35 USC § 112

2. Rejections are withdrawn in lifght of Applicant's amendments.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-10 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Computer Organization and Design (herein Hennessy) in view of Kawasaki (U.S. Patent No. 6,343,357).

5. Regarding claim 1, Hennessy discloses an overlapping command submitting method of dynamic cycle pipeline, for a chip having pipeline structure, comprising the following steps: (a) reading the command from a command buffer and storing it in a command register (Page 499: *reading from the instruction memory and storing in the IF/ID pipeline register*); (b) decoding the command (Page 499; Page 450 Decode stage); (c) preprocessing operators of the command (Page 469 Fig. 6.29), preparing initial operators of each stage of the pipeline, and storing them into a initialization register (Page 499 *storing in ID/EX pipeline register*); (d) judging whether the pipeline is not full, if it is not full (489-91 *absent a stall, new instruction is automatically inserted*)

Hennessy fails to disclose the remaining limitations.

Kawasaki discloses shared data transfer and instruction fetch buses as well as delaying the fetch until the data transfer is complete (Kawasaki Col. 4 lines 1-7).

Hennessy would have been motivated to used the shared bus to limit the cost of processor resources and to delay the fetch in order to "simplify either a processing when the data fetch and the instruction fetch conflict or a post-processing caused by the former" (Kawasaki col 4 lines 5-7).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Hennessy and incorporate the shared buses and the functionality of delaying the fetch of an instruction during a conflict. None in Hennessy, the final stage of the pipeline is the Write Back stage which writes data back to the register file. This may result in a conflict if there are shared buses used with instruction fetch. Therefore, to determine whether such a conflict exists, we have to wait until the processor indicates that a command is in the WB stage (remaining limitations of step (d)); then, judge whether there is a conflict, and if yes, waiting until the old command has exited (step (e)); or, otherwise, submitting the new command into the pipeline while it is in the last cycle (step (f)).

6. Regarding claim 4, Hennessy/Kawasaki discloses the command submitting method of Claim 1 wherein the exiting signal is released before two stages when the new command enters the pipeline stage (Kawasaki col 4 lines 1-7).

7. Regarding claim 5, Hennessy/Kawasaki discloses the command submitting method of Claim 1 wherein the command relevance means that the new command and the old command cannot share the hardware processing module in the same one pipeline stage (Kawasaki col 4 lines 1-5).

8. Regarding claim 6, Hennessy/Kawasaki discloses the command submitting method of Claim 1, wherein in the Step (e), it is also judged in which stage of the

pipeline field switch shall be conducted for the new and old commands, and the field switch is completed in the corresponding pipeline stage where the new and old commands overlaps (Kawasaki col 4 lines 1-7).

9. Regarding claim 7, Hennessy/Kawasaki discloses the command submitting method of Claim 1, wherein in the Step (e), it is also judged whether there is any field conflict between the new command and the old command, if there is, then the field of the new command is added into the pipeline when submitting, and the field of the old command enters into the field branch and maintains in the field brance until the last time that the old command uses this field; in case there is no field conflict, the field switch is conducted in the corresponding pipeline stage after submitting (Kawasaki col 4 lines 1-7)

10. Regarding claim 8, Hennessy/Kawasaki discloses the command submitting method of Claim 1, characterized wherein in the Step (c), it is required to provide the initial status of all kinds of commands at the entry to the pipeline (Page 469 Fig. 6.29 -- *every instruction has its initial status provided*).

11. Regarding claim 9, Hennessy/Kawasaki discloses the command submitting method of Claim 1, wherein the said commands include reading/writing memory commands (MIPs data transfer instructions), reading/writing control register commands (MIPs move instructions) and various searching commands (MIPs Arithmetic

Instructions that search for operands; *moreover, all instructions can be used as part of searching algorithms*).

12. Regarding claim 10, Hennessy/Kawasaki discloses the chip on which the method according to Claim 1, is carried out having the cycle pipeline structure, comprising: interface of host computer (Page 499), input buffer (IF/ID pipeline register), command processing unit (Control), and result unit (Write Back Stage); the command processing unit comprises: command interpreter (Multiplexers receiving control signals & ALU control) and pipeline performing unit (anything in 499); characterized in that the command interpreter further comprises: command buffer controllers (pipeline registers), command register (portion of IF/ID pipeline register holding opcodes), processing unit of operator (ALU control), pipeline initialization register and control automaton (EX/ME pipeline register/ALU control), which are connected in order; the control automaton controls the command buffer controller to read a command from the command buffer (ALU control completes this), and stores the command into the command register; the control automaton decodes the command (Decode stage), and controls the processing unit of operator to prepare initial operators of each pipeline stage according to the type of the command, and stores them into the pipeline initialization register (499).

13. Regarding claims 15-18, these claims are rejected for the same reason as claim 10.

14. Claims 2, 3, and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hennessy/Kawasaki in view of Vaglica (U.S. Patent No. 5,084,815).

15. Regarding claim 2, Hennessy/Kawasaki discloses thet method of Claim 1, but fails to disclose of an illegal instruction detector.

Vaglica discloses an illegal instruction detector and going to the next instruction if such a detection is made (col. 9 lines 48-68).

Hennessy/Kawasak would have been motivated to utilize this method to deal with illegal instructions that occur for a variety of reasons.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Hennessy/Kawasaki and incorporate the illegal instruction handler of Vaglica.

16. Regarding claim 3, Hennessy/Kawasaki/Vaglic discloses the command submitting method of Claim 2, wherein said illegal command includes: the instructions with incorrect command code and/or carrying unreasonable command parameters (Vaglica col. 9 lines 48-68 – *note that "and/or" is being interpreted as "or"*).

17. Regarding claims 10-14, these claims are rejected for the same reason as claim 10.

Response to Arguments

18. Applicant's arguments filed 18 March 2009 have been fully considered but they are not persuasive.

19. Applicant states:

> Hennessy fails to teach or suggest judging whether a pipeline is not full, if it is nol full, directly inserting a new command; otherwise, waiting for an exiting signal from a command in the pipeline in the last pipeline period before exiting, as required by claim 1. Instead, Hennessy discusses inserting at least one bubble into a pipeline when there is a conflict between an old instruction and a new instruction (see Hennessy, pages 489-91), and, as a result, bubbles may appear in the pipeline. In fact, the bubbles in Hennessy would cause problems similar to those discussed in the Background of tl~e Invention of the present application (see, e.g., the paragraph bridging pages 1 and 2 of the specification, among other places). Hennessy indeed provides no teaching or suggestion as to judging whether a pipeline is not full, if it is not full, directly inserting a new command; otherwise, waiting for an exiting signal from a command in the pipeline in the last pipeline period before exiting, much less any reason to expect that the advantages enjoyed by the present invention, e.g., efficient use of the pipeline, could be achieved.

Examiner disagrees. It is noted that this "bubble" refers to an NOP instruction being inserted into the pipeline. When the bubble is not required, there is a space in the fetch stage to execute a new instruction (i.e. the pipeline is not full). When this NOP instruction is required, it takes up the only location in which a new instruction may be submitted to the pipeline (i.e. the pipeline is full). The similarities to Applicant's prior art are not relevant to the appropriateness of the rejection. Indeed, if there is a distinction to be made distinguishing Applicant's prior art and preferred embodiment, such a distinction should be made clear in the claim language.

20. Applicant states:

> Kawasaki et al, is silent as to judging whether two commands are relevant. In fact, Kawasaki et al. provide no teaching or suggestion as to a need to judge whether two commands are relevant to each other because the pipe control is set to prefer the instruction fetch operation over the data transfer operation.

Examiner disagrees. The determination of relevancy in Hennessy/Kawasaki is the determination of whether there is a fetching/transferring conflict. If such a conflict exists, there is "relevance."

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRIAN P. JOHNSON whose telephone number is (571)272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brian Johnson/ Patent Examiner, Art Unit 2183

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183